LeWiz's Content Processor 5000™ is designed for ease of use in intelligent network equipment. Generally, these systems are known as layer 4-7 smart switches or network equipment that enable network managers to implement functions such as traffic prioritization, traffic shaping, bandwidth allocation, access control and load balancing. The Content Processor processes layer 3-7 information in the network packets and redirects or filters the packets to allow the system to perform intelligent network functions. The processor executes these functions in hardware allowing the network equipment to perform network functions with the least latency and highest performance.
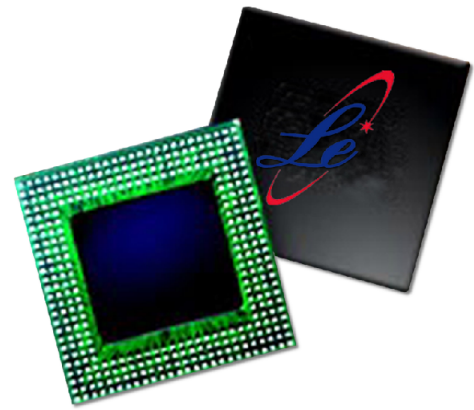
The content processor is implemented in deep sub-micron semiconductor technology. It consists of five major units: packet pre-processing, protocol parser, policy-based classifier, packet modification and forwarding engine, and system interface functions (See Figure 1).

Note: Three of these units are logically grouped together as the packet processor and will be described together as one block in Figure 1.

Features

- High performance, low latency
- Gigabit capability at line rate, non-blocking (OC-48 and higher)
- Process deep into layer 5-7 of packet - more intelligent switching, traffic management
- Providing XML capability for the upper layer processing, XML protocol handling
- URL switching
- Switching action based on upper layer parameters such as date, from, to, subject, content-type, etc.
- Fast forwarding of packet
- Perform table look up of connections
- Programmable protocol, policy, keyword extract
- Scalable in rules and data flows
- Support for persistent connection based on cookie, URL, source IP
- Support QoS, traffic prioritization
- Support load balancing based on rules
- Packet filtering, discard, re-direct based on rule or rule parameters
- Check and generate check sum, CRC
- Ease of interface to PCI with master and DMA capability
- Controlling fast external memory for storing packet data and traffic control information
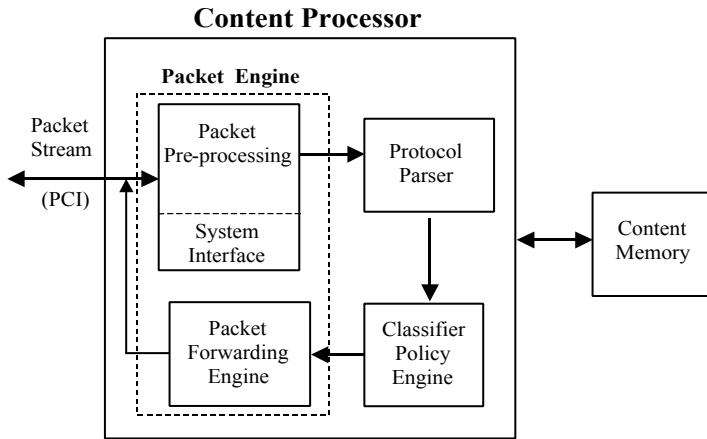- Support for server error interception and redirect
-
Delivery can be in the form of ASIC or as a PCI plug-in card
Available for SoC integration (Verilog based code)
Full software support with configuration and traffic management functions
Complete traffic management system reference design using the content processor is also available

Content Processor

Packet Engine

Packet Stream (PCI)

Packet Pre-processing

System Interface

Packet Forwarding Engine

Protocol Parser

Classifier Policy Engine

Content Memory

Packet processor

Three blocks of the content processor are grouped together and described below as the packet processor. These blocks include the system interface, the packet pre-processor, and the packet modification and forwarding engine.

The packet processor receives the packets from the external system bus and processes the layer 3-4 (TCP/IP) of the network data packets on the fly. It disassembles the packets and sends the upper layer information to the protocol parser for upper layer protocol processing. The processor handles TCP/IP session termination and does session table walks for tracking of TCP/IP connections.

The Content Processor 5000 interfaces to the external bus and controls the content processor's memory. The processor also controls the internal blocks of the content processor for the host to configure it.

After the upper layer information is processed and classified, the results are fed into the packet processor for editing the packet and forwarding the packet on to its determined destination with the right QoS. If the packet is to be discarded the packet processor removes it from the queue.

Protocol Parser

The protocol parser receives the layer 5-7 data from the packet processor. It feeds the data through selected upper layer protocol processing blocks and identifies keywords required for forming the query to search in the policy database of the classifier. The parser can support various protocols including string based protocols such as HTTP, ebXML or binary based upper layer protocols.

Classifier

The classifier is a large policy, rules engine. It contains the policy database for classifying network traffic per flow. Query rule parameters from the parser are fed into the classifier for searching in the database. The result is used to redirect traffic with pre-determined QoS assignment or discard the packet.

Packet processing block features:

- Layer 3-4 packet processing
  - Performs TCP/IP disassembly
  - TCP/IP session handling
  - Queuing of packets on the in-bound and the out-bound
  - Forwards layer 5-7 information to protocol parser
  - Edits the layer 3-4 information for fast forwarding of the packet
  - Reassembles the packet with the right QoS, destination
  - Generates new check sum, CRC
  - Discards the unwanted packets
- Capable of supporting millions of concurrent sessions
- Tracks traffic flow to perform session persistence and fast forwarding
- Terminates client accesses and handles server connections
- Interface to the internal blocks for configuration and error handling
- Interface to external content processor memory (fast pipeline ZBT SSRAMs)
- Interface to the system bus (64 bit, 66 MHz PCI) and communicate with the host processor

Protocol parser block features:

- Process upper layer protocols
- Supports: HTTP, SMTP, ebXML, NFS, CIFS and others
- Contains keyword look-up engine with programmable dictionary
- Fast extraction of string tags
- Fast search of string data
- Compose search query based on keywords and layer 3-4 information for the classification

Classifier block features:

- Deep policy database (16K policies)
- Classify traffic packets based on layer 3-7 information in hardware based on
  - TCP information such as source port, destination port
  - IP information such as source IP address, destination IP address
  - XML fields such as person name, action to be taken
  - URL, cookie information
  - etc.
- Produce results for
  - Packet redirect
  - Packet discard, or filter
  - Packet prioritization, QoS assignment
- Fast search in hardware